

JC978 U.S. PTO
10/028001



JC41958

U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL. NO.	FILING DATE	CLASS	SUBCLASS	CAV.	EXAMINER
0000001	12/03/01	3-5		0818	10-1-0
INVENTOR: Forbes Leonard; Eldridge Jerome; Ahn Kis; 2816					
**CONTINUING DATA-VERIFIED: THIS APPLICATION IS A CIP OF 09/943;134/08/30/2001 TR					
** FOREIGN APPLICATIONS VERIFIED:					
NO PUB. DO NOT PUBLISH <input type="checkbox"/> REASON <input type="checkbox"/>					
Foreign priority claimed		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no		ATTORNEY DOCKET NO.	
USC 110 conditions met		<input checked="" type="checkbox"/> yes <input type="checkbox"/> no		1303:035US1	
Verified and Acknowledged		Examiner's initials		DR	
TITLE: Programmable array logic or memory with pass channel devices and asymmetrical tunnel barriers U.S. DEPT. OF COMM. / PAT. & TM. PTO-4130 Rev. 12-94					
FORMAL DRAWINGS					

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NOTICE OF ALLOWANCE MAILED		TU TR HO Assistant Examiner 11/03		CLAIMS ALLOWED	
11/19/03				Total Claims 22	Print Claim for O.G. 1
ISSUE FEE				DRAWING	
Amount Due \$1630	Date Paid	David Neims Supervisory Patent Examiner Technology Center 2800 Primary Examiner		Sheets Drwg. 17	Figs. Drwg. 24
				Print Fig. 3	
<input type="checkbox"/> TERMINAL DISCLAIMER		PREPARED FOR ISSUE		Application Examiner	
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